US 20190280052A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2019/0280052 A1

FENG (43) Pub. Date: Sep. 12, 2019

(54) METHOD FOR MANUFACTURING A TOUCH-CONTROL PANEL AND OLED TOUCH-CONTROL APPARAUTS

(71) Applicant: **Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd.**, Wuhan (CN)

(72) Inventor: **Xiaoliang FENG**, Shenzhen (CN)

(21) Appl. No.: **16/102,764**

(22) Filed: **Aug. 14, 2018**

Related U.S. Application Data

(63) Continuation of application No. PCT/CN2018/087203, filed on May 17, 2018.

(30) **Foreign Application Priority Data**

Mar. 12, 2018 (CN) 201810201211.X

Publication Classification

(51) **Int. Cl.**

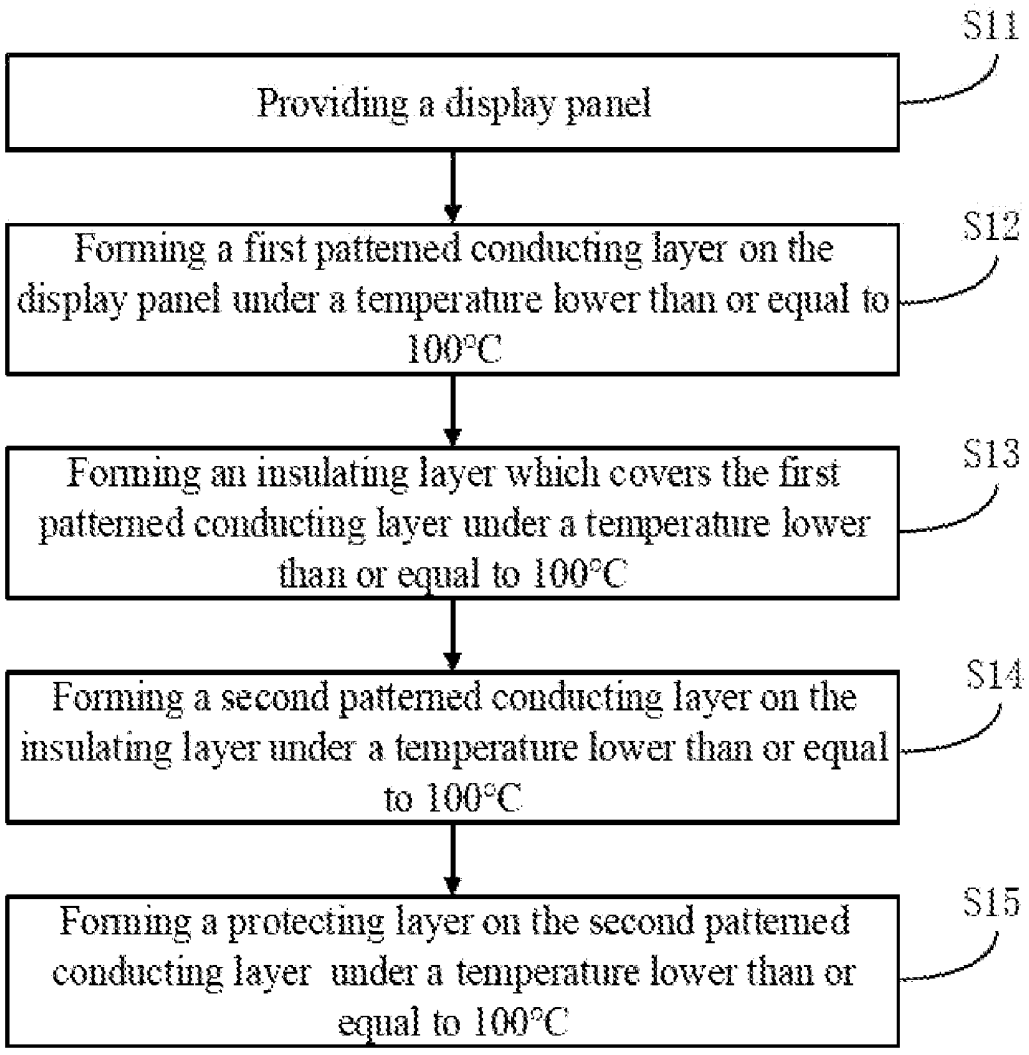
H01L 27/32	(2006.01)
G06F 3/041	(2006.01)
H01L 51/56	(2006.01)
H01L 51/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 27/323*** (2013.01); ***G06F 3/0412*** (2013.01); ***G06F 3/0416*** (2013.01); ***H01L 51/0005*** (2013.01); ***H01L 51/0023*** (2013.01); ***H01L 51/0097*** (2013.01); ***H01L 51/56*** (2013.01)

(57) **ABSTRACT**

The present disclosure provides a method for manufacturing a touch-control panel and a display apparatus. According to the method provided in the present disclosure, the touch-control panel may be manufactured under a temperature lower than or equal to 100° C. Therefore, the implementation of the present disclosure may avoid the problem of quality reduction of the touch-control structure due to high temperature, and thus improve the product yield.



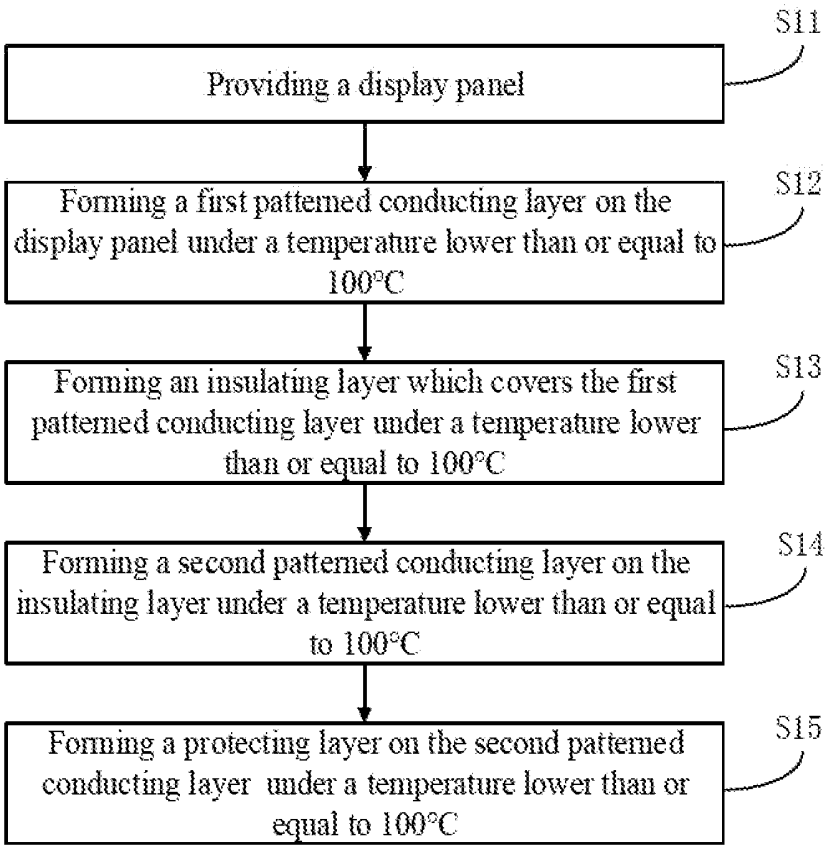

S11
Providing a display panel
S12
Forming a first patterned conducting layer on the display panel under a temperature lower than or equal to 100°C
S13
Forming an insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100°C
S14
Forming a second patterned conducting layer on the insulating layer under a temperature lower than or equal to 100°C
S15
Forming a protecting layer on the second patterned conducting layer under a temperature lower than or equal to 100°C

FIG. 1

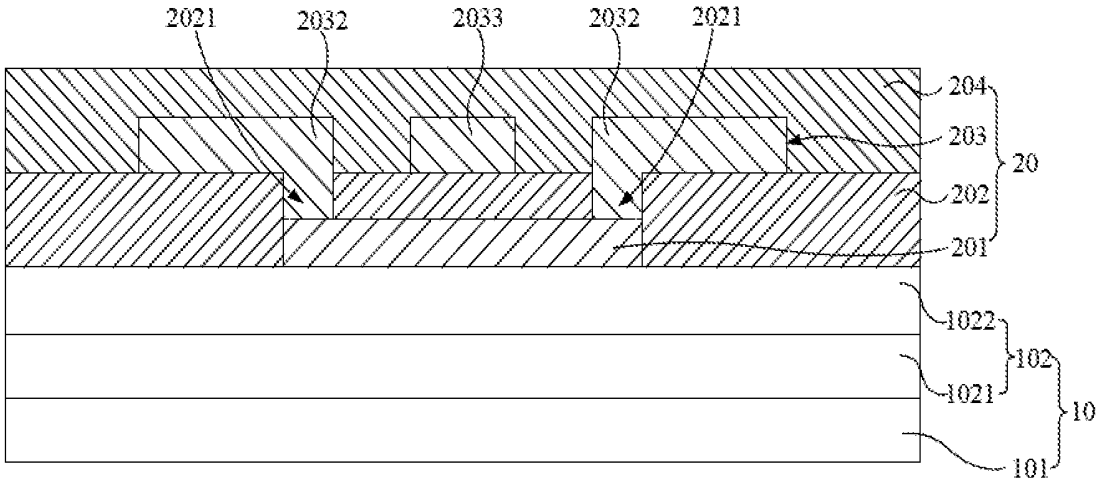

2021
2032
2033
2032
2021
204
203
202
201
20
1022
1021
102
10
101

FIG. 2

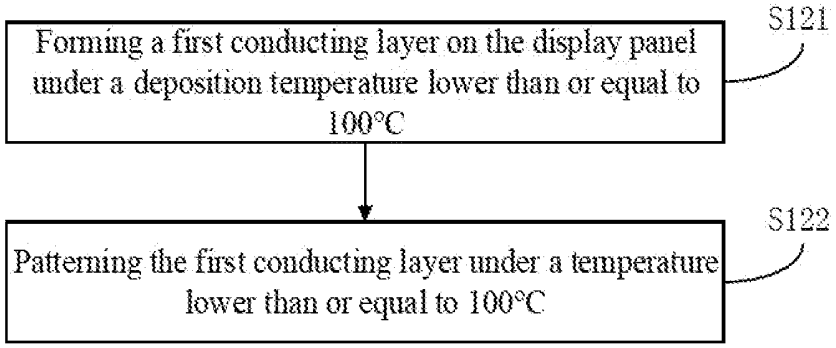


FIG. 3

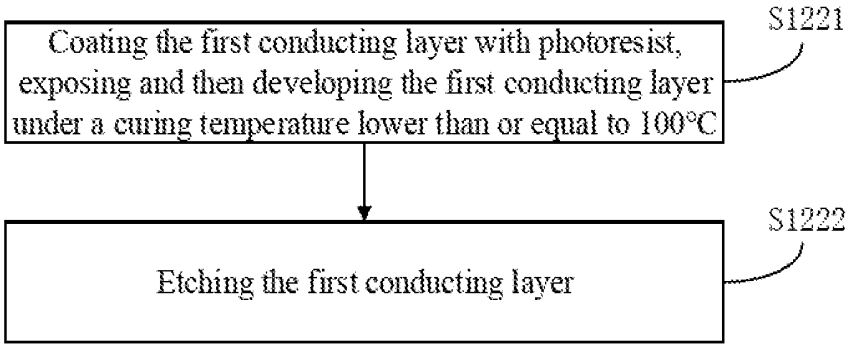


FIG. 4

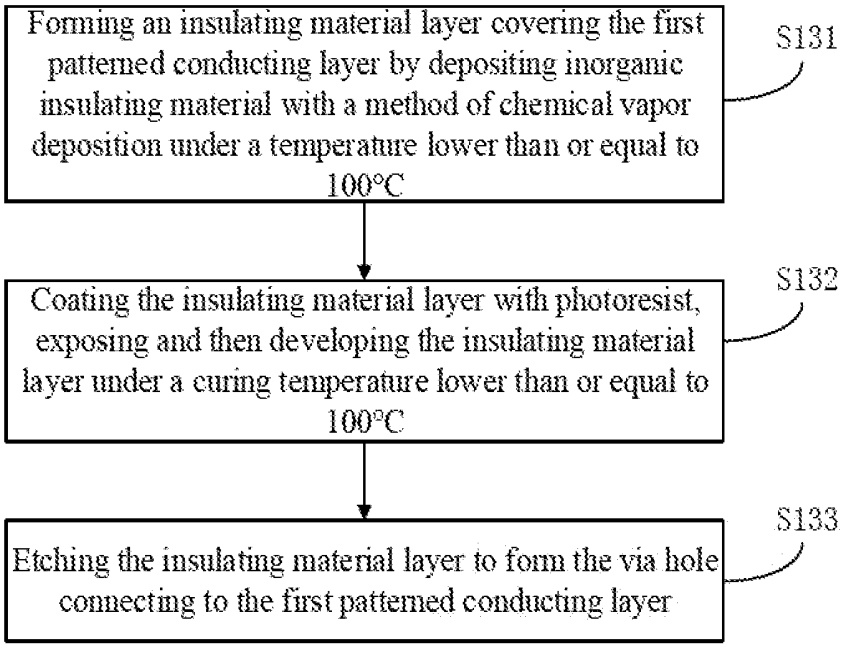


FIG. 5

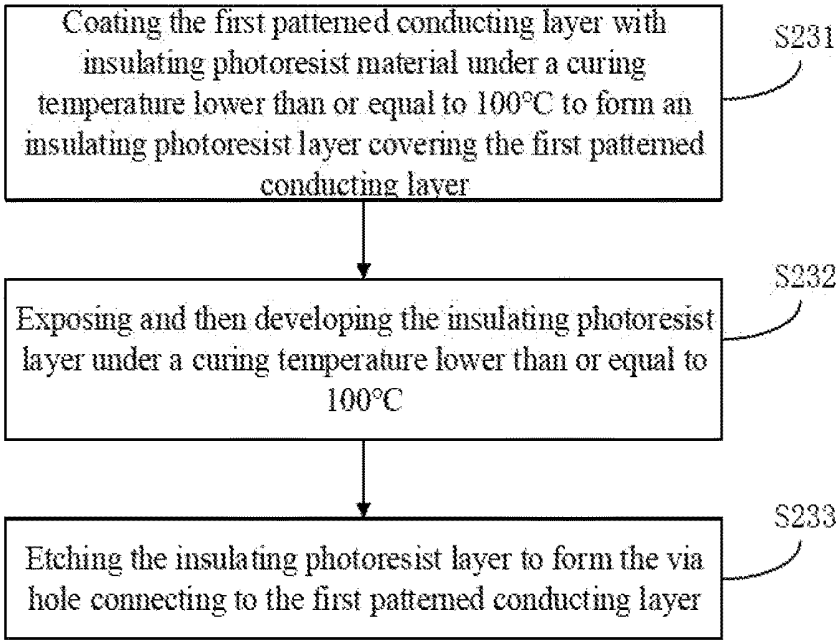


FIG. 6

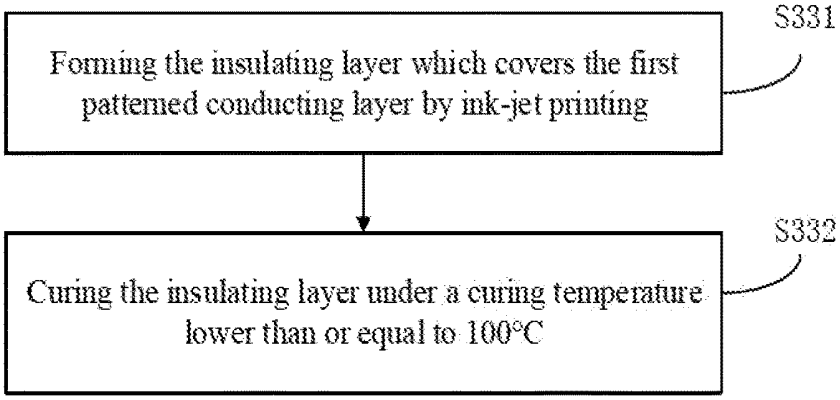


FIG. 7

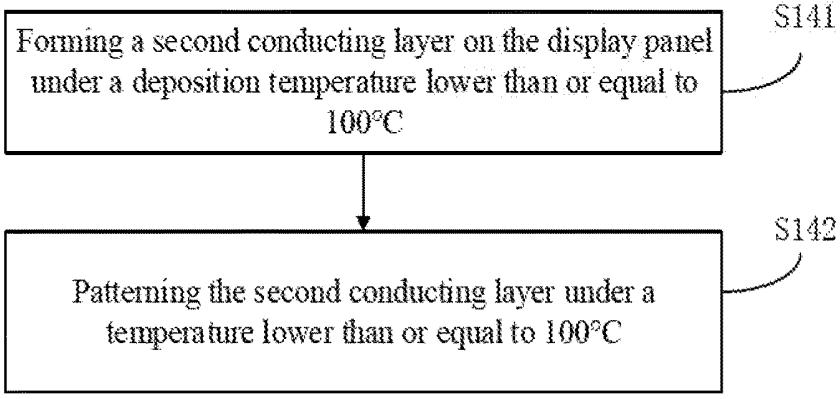


FIG. 8

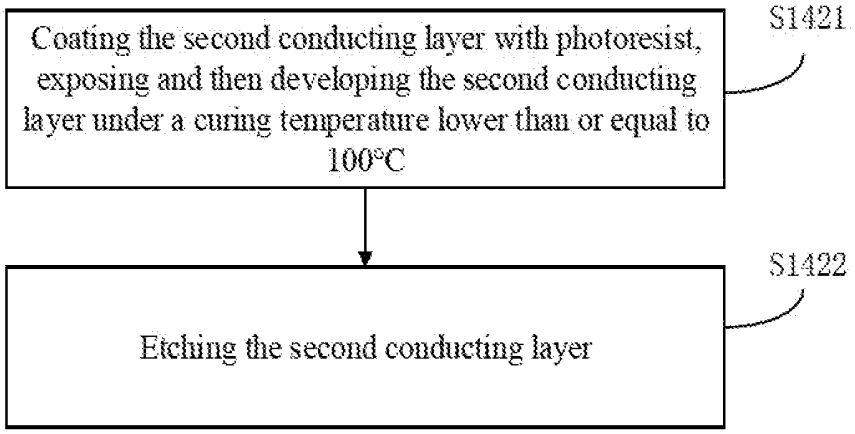

Coating the second conducting layer with photoresist, exposing and then developing the second conducting layer under a curing temperature lower than or equal to 100°C
S1421
Etching the second conducting layer
S1422

FIG. 9

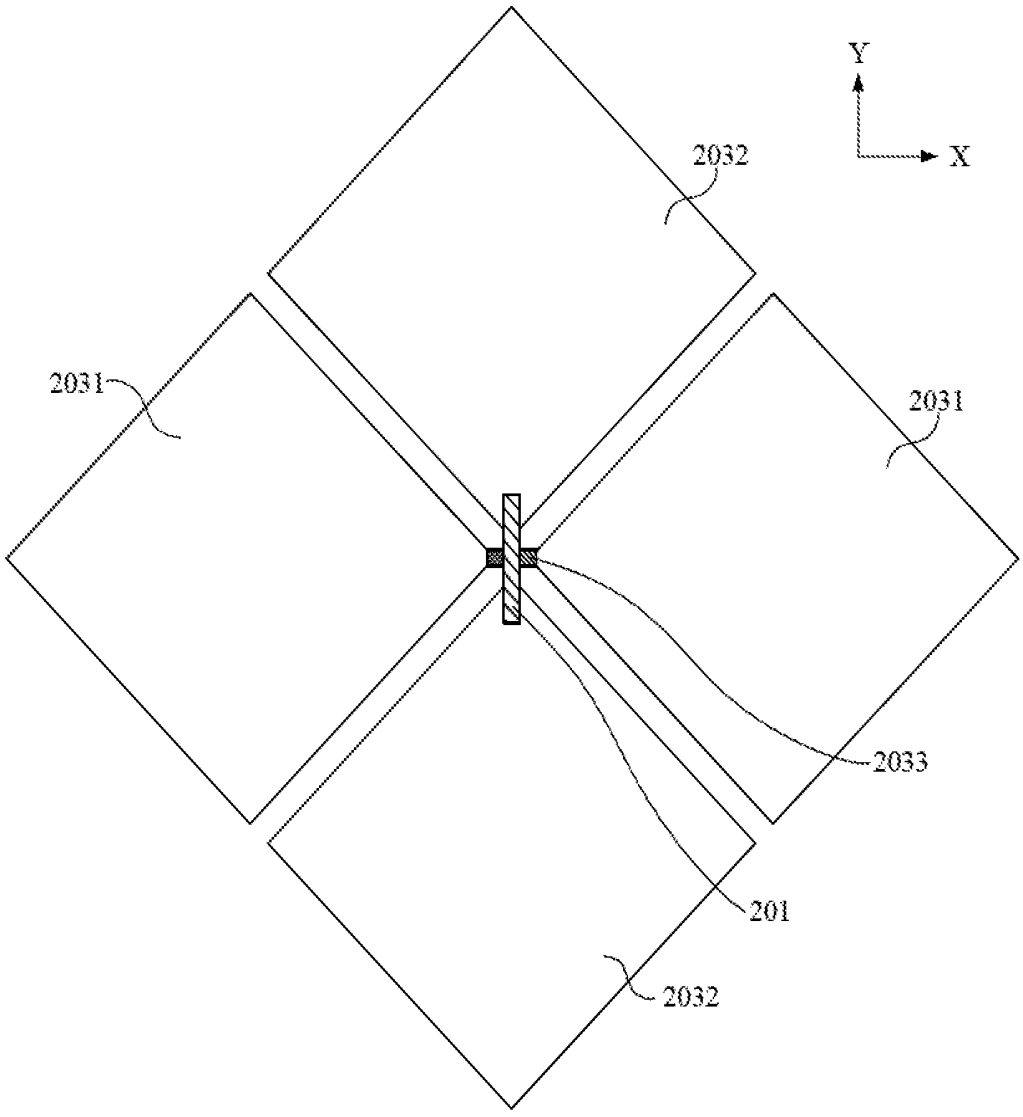

Y
X
2032
2031
2031
2033
201
2032

FIG. 10

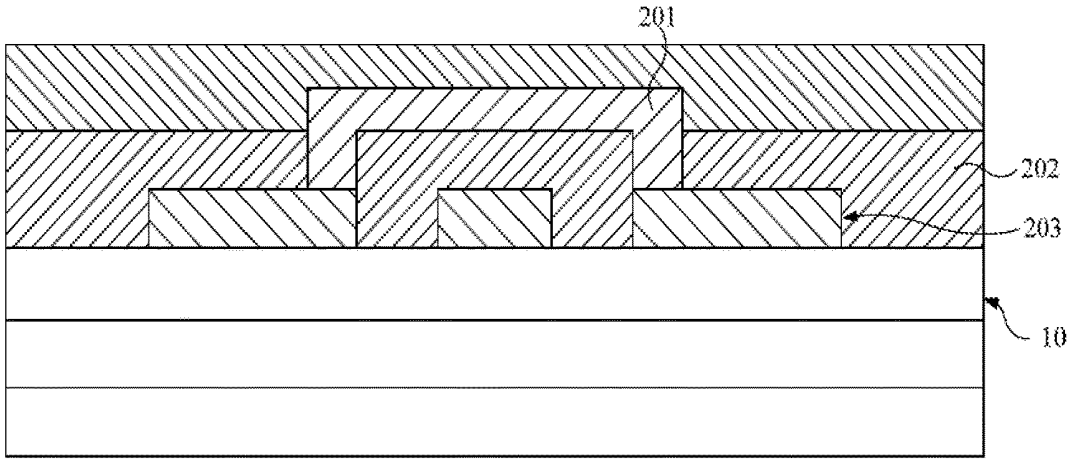

201
202
203
10

FIG. 11

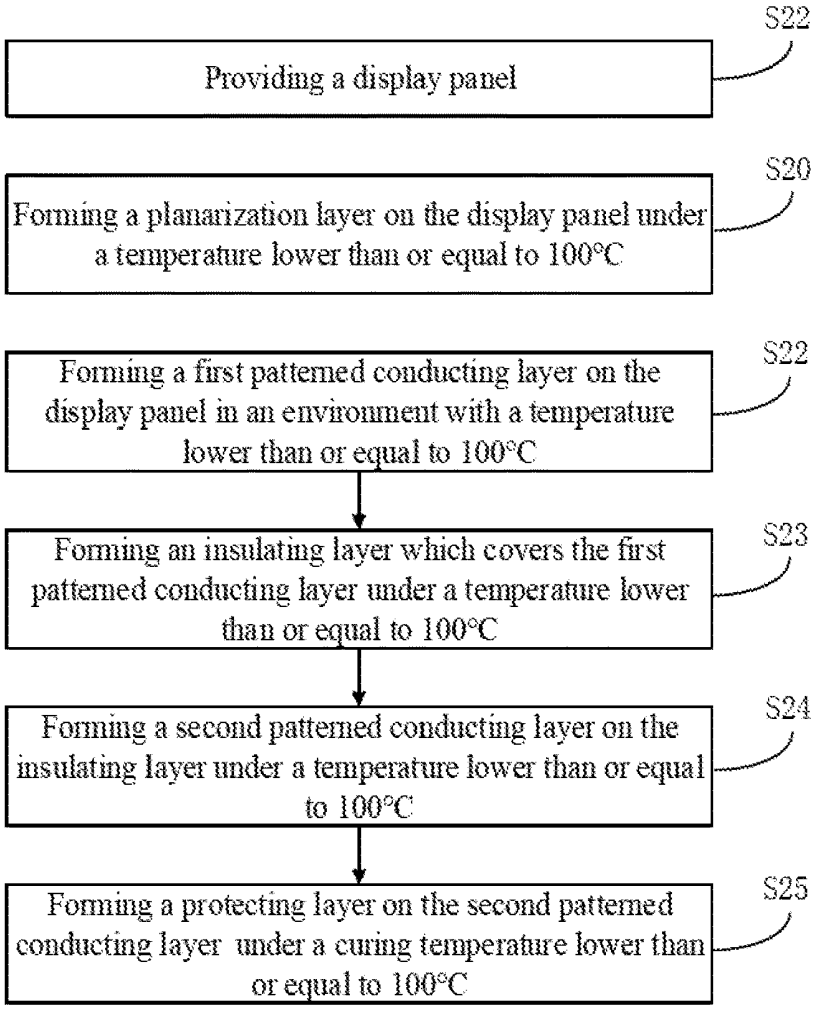

S22
Providing a display panel
S20
Forming a planarization layer on the display panel under a temperature lower than or equal to 100°C
S22
Forming a first patterned conducting layer on the display panel in an environment with a temperature lower than or equal to 100°C
S23
Forming an insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100°C
S24
Forming a second patterned conducting layer on the insulating layer under a temperature lower than or equal to 100°C
S25
Forming a protecting layer on the second patterned conducting layer under a curing temperature lower than or equal to 100°C

FIG. 12

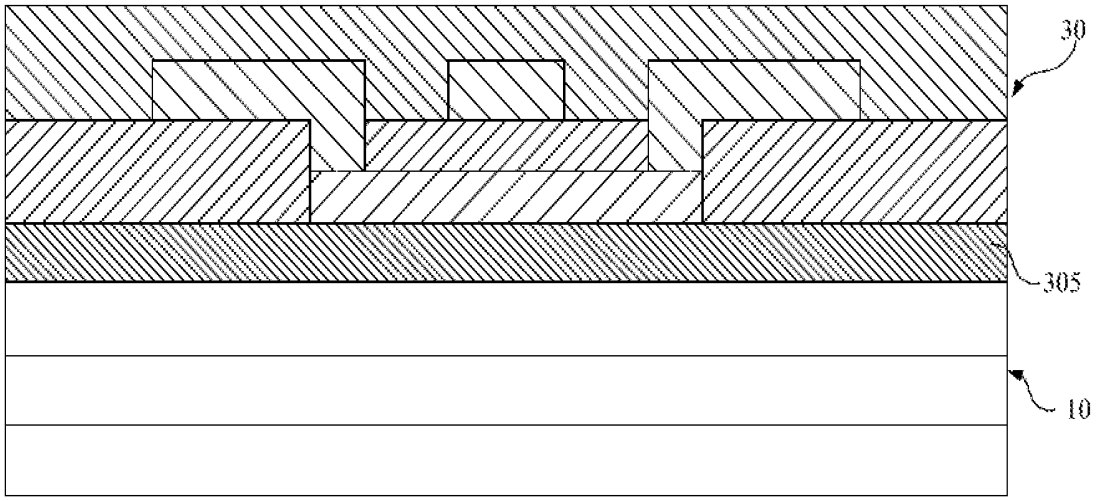


FIG. 13

METHOD FOR MANUFACTURING A TOUCH-CONTROL PANEL AND OLED TOUCH-CONTROL APPARAUTS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation-application of International (PCT) Patent Application No. PCT/CN2018/087203, filed on May 17, 2018, which claims foreign priority of Chinese Patent Application No. 201810201211.X, filed on Mar. 12, 2018 in the State Intellectual Property Office of China, the entire contents of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the display technique field, and in particular to a method for manufacturing a touch-control panel and an OLED touch-control display apparatus.

BACKGROUND

[0003] The organic light-emitting diode (OLED) cannot withstand high temperature. Thus, during the manufacturing of the touch-control layer of flexible OLED component, high manufacturing temperature may lead to a quality reduction of the touch-control panel, and thus reduce the product yield.

SUMMARY

[0004] Accordingly, the present disclosure aims to provide a provide a method for manufacturing a touch-control panel and an OLED touch-control display apparatus so as to solve the quality reduction and product yield reduction problem due to the high manufacturing temperature.

[0005] To solve the above mentioned problem, a technical scheme adopted by the present disclosure is to provide a method for manufacturing a touch-control panel. The method includes: providing a display panel; forming a first conducting layer on the display panel under a deposition temperature lower than or equal to 100° C.; patterning the first conducting layer under a temperature lower than or equal to 100° C. to form a first patterned conducting layer; forming an insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C., wherein the insulating layer defines a via hole connecting to the first patterned conducting layer; forming a second conducting layer on the insulating layer under a deposition temperature lower than or equal to 100° C.; and patterning the second conducting layer under a temperature lower than or equal to 100° C. and connecting the second patterned conducting layer with the first patterned connecting layer through the via hole of the insulating layer.

[0006] To solve the above mentioned problem, another technical scheme adopted by the present disclosure is to provide a method for manufacturing a touch-control panel. The method includes: providing a display panel; forming a first patterned conducting layer on the display panel under a temperature lower than or equal to 100° C.; forming an insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C., wherein the insulating layer defines a via hole connecting to the first patterned conducting layer, and forming a second patterned conducting layer on the insulating layer under a temperature lower than or equal to 100° C., wherein the second patterned conducting layer is connected with the first patterned conducting layer though the via hole.

[0007] To solve the above mentioned problem, another technical scheme adopted by the present disclosure is to provide an OLED touch-control display apparatus, comprising a touch-control panel with an OLED component, wherein the touch-control panel is manufactured by the above-mentioned method.

[0008] By the method of: providing a display panel; forming a first patterned conducting layer on the display panel under a temperature lower than or equal to 100° C.; forming an insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C., wherein the insulating layer defines a via hole connecting to the first patterned conducting layer, and forming a second patterned conducting layer on the insulating layer under a temperature lower than or equal to 100° C., the first patterned conducting layer and the second patterned conducting layer may be connected together through the via hole and the touch-control panel may be manufactured under a temperature lower than or equal to 100° C. Therefore, the implementation of the present disclosure may avoid the problem of quality reduction of the touch-control panel due to high temperature, and thus improve the product yield.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] In order to clearly explain the technical solutions in the embodiments of the present disclosure, the drawings used in the description of the embodiments will be briefly described below. Obviously, the drawings in the following description are merely some embodiments of the present disclosure. For those of ordinary skill in the art, other drawings may also be obtained based on these drawings without any creative work.

[0010] FIG. **1** is a flow chart of the method for manufacturing a touch-control panel according to an embodiment of the present disclosure.

[0011] FIG. **2** shows a schematic diagram of the OLED touch-control apparatus according to an embodiment of the present disclosure.

[0012] FIG. **3** shows the sub-blocks of the block S**12** of FIG. **1** according to an embodiment of the present disclosure.

[0013] FIG. **4** shows the sub-blocks of the block S**122** of FIG. **3** according to an embodiment of the present disclosure.

[0014] FIG. **5** shows the sub-blocks of the block S**13** of FIG. **1** according to an embodiment of the present disclosure.

[0015] FIG. **6** shows the sub-blocks of the block S**13** of FIG. **1** according to another embodiment of the present disclosure.

[0016] FIG. **7** shows the sub-blocks of the block S**13** of FIG. **1** according to yet another embodiment of the present disclosure.

[0017] FIG. **8** shows the sub-blocks of the block S**14** of FIG. **1** according to an embodiment of the present disclosure.

[0018] FIG. **9** shows the sub-blocks of the block S**142** of FIG. **8** according to an embodiment of the present disclosure.

[0019] FIG. **10** shows a schematic diagram of connection between the first patterned conducting layer and the second patterned conducting layer of FIG. **2**.

[0020] FIG. **11** shows a schematic diagram of the OLED touch-control apparatus according to another embodiment of the present disclosure.

[0021] FIG. **12** is a flow chart of the method for manufacturing a touch-control panel according to another embodiment of the present disclosure.

[0022] FIG. **13** shows a schematic diagram of the OLED touch-control apparatus according to another embodiment of the present disclosure.

DETAILED DESCRIPTION

[0023] The disclosure will now be described in detail with reference to the accompanying drawings and examples. Apparently, the described embodiments are only a part of the embodiments of the present disclosure, not all of the embodiments. All other embodiments obtained by a person of ordinary skill in the art based on the embodiments of the present invention without creative efforts shall fall within the protection scope of the present invention.

[0024] Referring to FIGS. **1** & **2**, FIG. **1** is the flow chart of the method for manufacturing the touch-control panel **20** according to an embodiment of the present disclosure. In this embodiment, the method may include the following blocks.

[0025] S**11**: Providing a display panel.

[0026] As shown in FIG. **2**, the display panel **10** may include a substrate **101** and a display unit **102**. The substrate **101** may be a flexible substrate, and may be made of organic material such as polyimide. The display unit **102** may include a thin-film transistor **1021** and an OLED component layer **1022**.

[0027] The thin film transistor **1021** may be an amorphous-silicon thin-film transistor, thin-film transistor with oxide or low temperature poly-silicon thin-film transistor.

[0028] S**12**: Forming a first patterned conducting layer under a temperature lower than or equal to 100° C.

[0029] Referring to FIG. **3**, the block S**12** may specifically include the following sub-blocks.

[0030] S**121**: Forming a first conducting layer on the display panel under a deposition temperature lower than or equal to 100° C.

[0031] Specifically, conducting material may be deposited on the OLED component layer **1022** by physical vapor deposition (PVD) so as to form the first conducting layer. The deposition temperature during the PVD process may be configured to be lower than or equal to 100° C.

[0032] Optionally, the conducting material may be at least one of, by way of example but not limited to, indium tin oxides (ITO), aluminum, copper, silver, titanium, molybdenum and their alloy.

[0033] S**122**: Patterning the first conducting layer under a temperature lower than or equal to 100° C.

[0034] Referring to FIG. **4**, the block S**122** may specifically include the following sub-blocks.

[0035] S**1221**: Coating the first conducting layer with photoresist, exposing and then developing the photoresist under a temperature lower than or equal to 100° C.

[0036] Specifically, the photoresist coating equipment may use spin coating technique. The rotation may make the photoresist agent dropped on the first conducting layer to spread. A photoresist membrane may be formed under the surface tension of the photoresist agent and the centrifugal force. After its formation, the photoresist membrane may be baked under a baking temperature lower than or equal to 100° C. so as to form a dry photoresist membrane, i.e., the photoresist layer.

[0037] The photoresist agent may be a photosensitive material which mainly consists of resin, photosensitive agent and solvent.

[0038] Furthermore, after the formation of the photoresist layer, the photoresist layer may be exposed under a mask. Then the exposed photoresist layer may be developed with developing solution. Then the photoresist layer may be baked and cured under a baking temperature lower than or equal to 100° C. Thus, the adhesion of the photoresist layer which has been softened and inflated during developing may be strengthened, and the corrosion resistance of the photoresist layer may be improved.

[0039] S**1222**: Etching the first conducting layer.

[0040] The first conducting layer may be etched in the sub-block S**1222**.

[0041] Specifically, wet etching with etching liquid may be applied to form the first patterned conducting layer **201**. Alternatively, dry etching of the first conducting layer under a temperature lower than or equal to 100° C. may be utilized to form the first patterned conducting layer **201**.

[0042] S**13**: Forming an insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C.

[0043] Referring to FIG. **5**, the block S**13** may specifically include the following sub-blocks.

[0044] S**131**: Forming an insulating material layer covering the first patterned conducting layer by depositing inorganic insulating material with a method of chemical vapor deposition (CVP) under a temperature lower than or equal to 100° C.

[0045] Optionally, the insulating material may be at least one of silicon nitride or silicon oxide.

[0046] S**132**: Coating the insulating material layer with photoresist, exposing and then developing the photoresist under a curing temperature lower than or equal to 100° C.

[0047] Specifically, the photoresist coating equipment may use spin coating technique. The rotation may make the photoresist agent dropped on the insulating material layer to spread. A photoresist membrane may be formed under the surface tension of the photoresist agent and the centrifugal force. After its formation, the photoresist membrane may be baked under a baking temperature lower than or equal to 100° C. so as to form a dry photoresist membrane, i.e., the photoresist layer.

[0048] The photoresist agent may be a photosensitive material which consists of resin, photosensitive agent and solvent.

[0049] Furthermore, after the formation of the photoresist layer, the photoresist layer may be exposed under a mask. Then the exposed photoresist layer may be developed with developing solution. Then the photoresist layer may be baked and cured under a baking temperature lower than or equal to 100° C. Thus, the adhesion of the photoresist layer which has been softened and inflated during developing may be strengthened, and the corrosion resistance of the photoresist layer may be improved.

[0050] S**133**: Etching the insulating material layer to form the via hole connecting to the first patterned conducting layer.

[0051] The insulating layer may be etched in the sub-block S**133**. Specifically, wet etching with etching liquid may be applied to form the insulating layer **202** with the via hole **2021**. Alternatively, dry etching of the insulating material layer under a temperature lower than or equal to 100° C. may be utilized to form the insulating layer **202** with the via hole **2021**.

[0052] Referring to FIG. **6**, in another embodiment, the block S**13** may specifically include the following sub-blocks.

[0053] S**231**: Coating the first patterned conducting layer with insulating photoresist material under a curing temperature lower than or equal to 100° C. to form an insulating photoresist layer covering the first patterned conducting layer.

[0054] Specifically, the photoresist coating equipment may use spin coating technique to coat and cover the first patterned conducting layer **201** with insulating photoresist material to form the insulating photoresist membrane. After its formation, the insulating photoresist membrane may be baked under a baking temperature lower than or equal to 100° C. so as to form a dry insulating photoresist membrane, i.e., the insulating photoresist layer.

[0055] S**232**: Exposing and then developing the insulating photoresist layer under a curing temperature lower than or equal to 100° C.

[0056] Specifically, after the formation of the insulating photoresist layer, the insulating photoresist layer may be exposed under a mask. Then the exposed insulating photoresist layer may be developed with developing solution. Then the insulating photoresist layer may be baked and cured under a baking temperature lower than or equal to 100° C. Thus, the adhesion of the insulating photoresist layer which has been softened and inflated during developing may be strengthened, and the corrosion resistance of the photoresist layer may be improved.

[0057] S**233**: Etching the insulating photoresist layer to form the via hole connecting to the first patterned conducting layer.

[0058] The insulating photoresist layer may be etched in the sub-block S**233**. Specifically, wet etching with etching liquid may be applied to form the insulating layer **202** with the via hole **2021**. Alternatively, dry etching of the insulating material layer under a temperature lower than or equal to 100° C. may be utilized to form the insulating layer **202** with the via hole **2021**.

[0059] In sub-blocks S**231** to S**233**, the insulating photoresist material may be directly coated onto the first patterned conducting layer, then exposed and developed to form the insulating layer **202**. Compared with the method of firstly depositing inorganic insulating material and then performing coating, exposing, developing and etching to form the insulating layer **202**, this method requires less processing steps. Thus, the embodiment may reduce the cost of the process.

[0060] Referring to FIG. **7**, in another embodiment, the block S**13** may specifically include the following sub-blocks.

[0061] S**331**: Forming the insulating layer which covers the first patterned conducting layer by ink-jet printing.

[0062] Specifically, the insulating layer **202** which covers the first patterned conducting layer **201** and defines the via hole **2021** connecting to the first patterned conducting layer **201** may be directly printed out. Thus, the steps of deposition, photoresist coating, exposing, developing and etching may be omitted, and the cost of the process may be reduced.

[0063] S**332**: Curing the insulating layer under a curing temperature lower than or equal to 100° C.

[0064] Specifically, after the insulating layer **202** is directly printed out. The insulating layer **202** may be baked and cured under a baking temperature lower than or equal to 100° C. Alternatively, the insulating layer **202** may be cured by light under a light-curing temperature lower than or equal to 100° C.

[0065] S**14**: Forming a second patterned conducting layer on the insulating layer under a temperature lower than or equal to 100° C.

[0066] Referring to FIG. **8**, the block S**14** may specifically include the following sub-blocks.

[0067] S**141**: Forming a second conducting layer on the insulating layer under a temperature lower than or equal to 100° C.

[0068] Specifically, the second conducting layer may be formed by depositing conducting material on the insulating layer **202** by physical vapor deposition under a temperature lower than or equal to 100° C.

[0069] Optionally, the conducting material may be at least one of, by way of example but not limited to, indium tin oxides (ITO), aluminum, copper, silver, titanium, molybdenum and their alloy.

[0070] S**142**: Patterning the second conducting layer under a temperature lower than or equal to 100° C.

[0071] Referring to FIG. **9**, the block S**142** may include the following sub-blocks.

[0072] S**1421**: Coating the second conducting layer with photoresist, exposing and then developing the photoresist under a curing temperature lower than or equal to 100° C.

[0073] Specifically, the photoresist coating equipment may use spin coating technique. The rotation may make the photoresist agent dropped on the second conducting layer to spread. A photoresist membrane may be formed under the surface tension of the photoresist agent and the centrifugal force. After its formation, the photoresist membrane may be baked under a baking temperature lower than or equal to 100° C. so as to form a dry photoresist membrane, i.e., the photoresist layer.

[0074] The photoresist agent may be a photosensitive material which consists of resin, photosensitive agent and solvent.

[0075] Moreover, after the formation of the photoresist layer, the photoresist layer may be exposed under a mask. Then the exposed photoresist layer may be developed with developing solution. Then the photoresist layer may be baked and cured under a baking temperature lower than or equal to 100° C. Thus, the adhesion of the photoresist layer which has been softened and inflated during developing may be strengthened, and the corrosion resistance of the photoresist layer may be improved.

[0076] S**1422**: Etching the second conducting layer.

[0077] The second conducting layer may be etched in the sub-block S**1422**. Specifically, wet etching with etching liquid may be applied to form the second patterned conducting layer **203**. Alternatively, dry etching of the second conducting layer under a temperature lower than or equal to 100° C. may be utilized to form the second patterned conducting layer **201**.

[0078] Moreover, the second patterned conducting layer **203** may connect to the first patterned conducting layer **201** though the via hole **2021** of the insulating layer **202**.

[0079] Referring FIGS. **2** & **10**, the second patterned conducting layer **203** formed by etching the second conducting layer in block S**1422** may include several first patterned conducting sub-layers **2031** arranged along a first direction, several second patterned conducting sub-layers **2032** arranged along a second direction and a patterned connecting layer **2033**. In the embodiment of FIG. **10**, the first patterned conducting sub-layers **2031** may be arranged along the X direction while the second patterned conducting sub-layers **2032** may be arranged along the Y direction.

[0080] The first patterned conducting layer **201** may connect either the first patterned conducting sub-layers **2031** along the first direction or the second patterned conducting sub-layers **2032** along the second direction. The patterned connecting layer **2033** may correspondingly connect either the second patterned conducting sub-layers **2032** long the second direction or the first patterned conducting sub-layers **2031** along the first direction. In the figure of this embodiment, the first patterned conducting layer **201** may connect several second patterned conducting layer **2032** along the Y direction. The patterned connecting layer **2033** may connect several first patterned conducting sub-layers **2031** along the X direction.

[0081] Referring to FIG. **11**, in other embodiments, the order to perform the block S**14** and S**12** may be exchanged. In other word, the second patterned conducting layer **203** may be firstly formed on the display panel **10**, and then the first patterned conducting layer **201** connecting to the second patterned conducting layer **203** may be formed on the insulating layer **202**. The manufacturing process may be similar with those set forth in above embodiments and will not be described hereon.

[0082] Furthermore, the method of this embodiment may further include the following block.

[0083] S**15**: Forming a protecting layer on the second patterned conducting layer under a curing temperature lower than or equal to 100° C.

[0084] Specifically, the protecting layer **204** may be formed by coating the second patterned conducting layer **202** with photoresist, exposing and then developing the photoresist by a yellow-light photolithography process under a curing temperature lower than or equal to 100° C. Optionally, the protecting layer **204** may be an organic protecting layer.

[0085] In other embodiments, the protecting layer **204** may be printed onto the second patterned conducting layer **203** by ink-jet printing. After being printed out, the protecting layer **204** may be baked and cured under a baking temperature lower than or equal to 100° C. Alternatively, the protecting layer **204** may cured by light under a light-curing temperature lower than or equal to 100° C.

[0086] Referring to FIGS. **12** & **13**, FIG. **12** shows the flow chart of the method for manufacturing the touch-control panel **30** according to another embodiment of the present disclosure. The blocks S**21**, S**22**. S**23**, S**24** and S**25** are similar to the blocks S**11**, S**12**, S**13**, S**14** and S**15** of the above-mentioned embodiments and will not be described hereon. In this embodiment, after the block S**21**, the method may further include:

[0087] S**20**: Forming a planarization layer on the display panel under a temperature lower than or equal to 100° C.

[0088] As shown in FIG. **13**, the planarization layer **305** may be formed on the display panel **10** by physical vapor deposition. The deposition temperature during the PVD process may be configured to be lower than or equal to 100° C.

[0089] Optionally, the planarization layer **305** may be an inorganic planarization layer made of silicon nitride or silicon oxide, or alternative an organic planarization.

[0090] Moreover, referring to FIGS. **2** & **13**, the present disclosure may further provide an OLED touch-control display apparatus. The apparatus may include a touch-control structure with an OLED component **10**.

[0091] The touch-control panel may be manufactured according to any one of the above-described embodiments, e.g., the touch-control panel **20** or **30**. Detailed description may be found in the above-mentioned embodiments and will not be described hereon.

[0092] By the method of: providing a display panel: forming a first patterned conducting layer on the display panel under a temperature lower than or equal to 100° C.; forming an insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C., wherein the insulating layer defines a via hole connecting to the first patterned conducting layer; and forming a second patterned conducting layer on the insulating layer under a temperature lower than or equal to 100° C., the first patterned conducting layer and the second patterned conducting layer may be connected together through the via hole and the touch-control panel may be manufacturing under a temperature lower than or equal to 100° C. Therefore, the implementation of the present disclosure may avoid the problem of quality reduction of the touch-control panel due to high temperature, and thus improve the product yield.

[0093] The foregoing is merely embodiments of the present disclosure, and is not intended to limit the scope of the disclosure. Any transformation of equivalent structure or equivalent process which uses the specification and the accompanying drawings of the present disclosure, or directly or indirectly application in other related technical fields, are likewise included within the scope of the protection of the present disclosure.

What is claimed is:

1. A method for manufacturing a touch-control panel, comprising:

providing a display panel;

forming a first conducting layer on the display panel under a deposition temperature lower than or equal to 100° C.;

patterning the first conducting layer under a temperature lower than or equal to 100° C. to form a first patterned conducting layer;

forming an insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C., wherein the insulating layer defines a via hole connecting to the first patterned conducting layer;

forming a second conducting layer on the insulating layer under a deposition temperature lower than or equal to 100° C.; and

patterning the second conducting layer under a temperature lower than or equal to 100° C. and connecting the second patterned conducting layer with the first patterned connecting layer through the via hole of the insulating layer.

2. The method of claim 1, wherein the patterning the first conducting layer under a temperature lower than or equal to 100° C. comprises:

coating the first conducting layer with photoresist, exposing and then developing the photoresist under a curing temperature lower than or equal to 100° C.; and

etching the first conducting layer by dry etching or wet etching under an etching temperature lower than or equal to 100° C.

3. The method of claim 1, wherein the forming the insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C. comprises:

forming an insulating material layer covering the first patterned conducting layer by depositing inorganic insulating material with a method of chemical vapor deposition under a temperature lower than or equal to 100° C.;

coating the insulating material layer with photoresist, exposing and then developing the photoresist under a curing temperature lower than or equal to 100° C.; and

etching the insulating material layer by dry etching or wet etching under an etching temperature lower than or equal to 100° C. to form the via hole connecting to the first patterned conducting layer.

4. The method of claim 1, wherein the forming the insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C. comprises:

coating the first patterned conducting layer with insulating photoresist material to form an insulating photoresist layer covering the first patterned conducting layer;

exposing and then developing the insulating photoresist material under a curing temperature lower than or equal to 100° C.; and

etching the insulating photoresist layer by dry etching or wet etching under an etching temperature lower than or equal to 100° C. to form the via hole connecting to the first patterned conducting layer.

5. The method of claim 1, wherein the forming the insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C. comprises:

forming the insulating layer which covers the first patterned conducting layer by ink-jet printing; and

curing the insulating layer under a curing temperature lower than or equal to 100° C.

6. The method of claim 1, wherein the patterning the second conducting layer under a temperature lower than or equal to 100° C. comprises:

coating the second conducting layer with photoresist, exposing and then developing the photoresist under a curing temperature lower than or equal to 100° C.; and

etching the second conducting layer by dry etching or wet etching under an etching temperature lower than or equal to 100° C.

7. The method of claim 1, further comprising:

forming a protecting layer on the second patterned conducting layer under a temperature lower than or equal to 100° C.

8. A method for manufacturing a touch-control panel, comprising:

providing a display panel;

forming a first patterned conducting layer on the display panel under a temperature lower than or equal to 100° C.;

forming an insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C., wherein the insulating layer defines a via hole connecting to the first patterned conducting layer; and

forming a second patterned conducting layer on the insulating layer under a temperature lower than or equal to 100° C., wherein the second patterned conducting layer is connected with the first patterned conducting layer though the via hole.

9. The method of claim 8, wherein the forming the first patterned conducting layer on the display panel under a temperature lower than or equal to 100° C. comprises:

forming a first conducting layer on the display panel under a deposition temperature lower than or equal to 100° C.; and

patterning the first conducting layer under a temperature lower than or equal to 100° C.

10. The method of claim 9, wherein the patterning the first conducting layer under a temperature lower than or equal to 100° C. comprises:

coating the first conducting layer with photoresist, exposing and then developing the photoresist under a curing temperature lower than or equal to 100° C.; and

etching the first conducting layer by dry etching or wet etching under an etching temperature lower than or equal to 100° C.

11. The method of claim 8, wherein the forming the insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C. comprises:

forming an insulating material layer covering the first patterned conducting layer by depositing inorganic insulating material with a method of chemical vapor deposition under a temperature lower than or equal to 100° C.;

coating the insulating material layer with photoresist, exposing and then developing the photoresist under a curing temperature lower than or equal to 100° C.; and

etching the insulating material layer by dry etching or wet etching under an etching temperature lower than or equal to 100° C. to form the via hole connecting to the first patterned conducting layer.

12. The method of claim 8, wherein the forming the insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C. comprises:

coating the first patterned conducting layer with insulating photoresist material under a curing temperature lower than or equal to 100° C. to form an insulating photoresist layer covering the first patterned conducting layer,

exposing and then developing the insulating photoresist layer under a curing temperature lower than or equal to 100° C.; and

etching the insulating photoresist layer by dry etching or wet etching under an etching temperature lower than or equal to 100° C. to form the via hole connecting to the first patterned conducting layer.

13. The method of claim **8**, wherein the forming the insulating layer which covers the first patterned conducting layer under a temperature lower than or equal to 100° C. comprises:

forming the insulating layer which covers the first patterned conducting layer by ink-jet printing; and

curing the insulating layer under a curing temperature lower than or equal to 100° C.

14. The method of claim **8**, wherein the forming the second patterned conducting layer on the display panel under a temperature lower than or equal to 100° C. comprises:

forming a second conducting layer on the display panel under a deposition temperature lower than or equal to 100° C.; and

patterning the second conducting layer under a temperature lower than or equal to 100° C. and connecting the second patterned conducting layer with the first patterned connecting layer through the via hole of the insulating layer.

15. The method of claim **14**, wherein the patterning the second conducting layer under a temperature lower than or equal to 100° C. comprises:

coating the second conducting layer with photoresist, exposing and then developing the photoresist under a curing temperature lower than or equal to 100° C.; and

etching the second conducting layer by dry etching or wet etching under an etching temperature lower than or equal to 100° C.

16. The method of claim **8**, further comprising:

forming a protecting layer on the second patterned conducting layer under a temperature lower than or equal to 100° C.

17. An OLED touch-control display apparatus, comprising a touch-control panel with an OLED component, wherein the touch-control panel is manufactured by the above-mentioned method.

* * * * *

专利名称(译)	触控面板的制造方法及OLED触控装置		
公开(公告)号	US20190280052A1	公开(公告)日	2019-09-12
申请号	US16/102764	申请日	2018-08-14
[标]发明人	FENG XIAOLIANG		
发明人	FENG, XIAOLIANG		
IPC分类号	H01L27/32 G06F3/041 H01L51/56 H01L51/00		
CPC分类号	H01L51/0097 H01L51/0023 H01L51/56 G06F3/0416 H01L27/323 G06F3/0412 H01L51/0005 G06F3/0443 G06F3/0446 G06F2203/04103 G06F2203/04111		
优先权	201810201211.X 2018-03-12 CN		
外部链接	Espacenet USPTO		

摘要(译)

本公开提供了一种用于制造触摸控制面板的方法和显示装置。根据本发明提供的方法，可以在低于或等于100℃的温度下制造触控面板。因此，本发明的实施可以避免触控质量下降的问题。结构由于高温，从而提高了产品产量。